REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-11. Specifically, the Office Action rejected claim 1-11 under 35 U.S.C. 102(b) as being unpatentable over Crouch (U.S. Patent No.5,592,493, "Crouch" hereinafter). Applicants have amended claims 1 and 6. After entry of the foregoing amendments, claims 1-11 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Examiner's Interview

After a telephone interview between the undersigned and the Examiner Trimmings, it was indicated that:

1. The added limitation of "providing a test pattern through a plurality of input lines" is not fully supported by the original disclosure. Fig.3 shows five inputs (inputs 1-5). However, the only description of input 1-5 appears on page 7, lines 4-6:"The clock terminal CLK of the MUX finite state machine controller 316 receives a clock signal, and the input terminals (input 1 to input 5) thereof receives the corresponding data or commands." There is no specific description indicating that the test pattern is provided through a plurality of input lines. The "corresponding data or commands" is too broad and may include data other than a test pattern.
2. The argument that "the registers of the present invention are not serially connected to each other" are not supported because of no specific disclosure in the specification.

Applicants do not agree with the assertions set forth above and respectfully traverse the rejections for at least the reasons set forth below.

The feature of "providing a test pattern through a plurality of input lines" is well supported

MPEP 2163 provides a well-established guideline in the evaluation of any patent application for compliance with the written description requirement of 35 U.S.C. 112.

> As stated, an applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997).
>
> It is clearly defined that "the analysis of whether the specification complies with the written description requirement calls for the examiner to compare the scope of the claim with the scope of the description to determine whether applicant has demonstrated possession of the claimed invention. Such a review is conducted from the standpoint of one of skill in the art at the time the application was filed (see, e.g., *Wang Labs. v. Toshiba Corp.*, 993 F.2d 858, 865, 26 USPQ2d 1767, 1774 (Fed. Cir. 1993)) and should include a determination of the field of the invention and the level of skill and knowledge in the art. Generally, there is an inverse correlation between the level of skill and knowledge in the art and the specificity of disclosure necessary to satisfy the written description requirement. Information which is well known in the art need not be described in detail in the specification. See, e.g., *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379-80, 231 USPQ 81, 90 (Fed. Cir. 1986).

The newly added feature of "providing a test pattern through a plurality of input lines" is well supported in the Figures 3 and 4. As shown in Figure 3, the intellectual product circuit module 302 receives the synchronous clock signal from the MUX finite state machine controller 316 for test activating. As also supported in the disclosure on page 7, lines 10-14, which stated as followed:

> "the MUX finite state machine controller 316 asserts a test activating signal, such as synchronous clock signal to the synchronous clock terminal of the intellectual product circuit module 302. The intellectual product circuit module 302 is then operated and tested in a time division way according to the stored test patterns in the registers 310, 312 and 314."

People skilled in the art at the time the application was filed would understand that the "MUX finite state machine controller" is used to control the input 1~input 5 for providing a test pattern in a parallel manner and control the test pattern, in a time division way, to be stored in the register 310 coupled to ENR1 signal, to be stored in the register 312 coupled to ENR2 signal, and to be stored in the register 314 coupled to ENR3 signal. Then, the MUX finite state machine controller control the intellectual product circuit module 302 by the synchronous clock signal to be operated and tested with the test pattern from the enabled registers.

The description of inputs 1-5 appears on page 7, lines 4-6: "The clock terminal CLK of the MUX finite state machine controller 316 receives a clock signal, and the input terminals (input 1 to input 5) thereof receives the corresponding data or commands" well supports the newly added feature of "providing a test pattern through a plurality of input lines." If the inputs 1-5 are not used for providing a test pattern, it is not necessary to specifically point out the multiple input pins as input 1 ~ input 5 in the drawing, instead, one input pin is required for serially input the test pattern. The analysis of whether the specification complies with the written description requirement should be conducted from the standpoint of one of skill in the art at the time the application was filed.

As shown in Figure 4, the intellectual product circuit modules 406, 408 and 410 respectively receive the synchronous clock signals A, B and C from the MUX finite state machine controller 418 for test activating. People skilled in the art at the time the application was filed would understand that the "MUX finite state machine controller" is used to control multiple inputs for providing a test pattern in a parallel manner, and control the test pattern, in a time division way, to be buffered in the register 420, the register 422, and the register 424. Then, the MUX finite state machine controller control the intellectual product circuit modules 406, 408 and 410 by the synchronous clock signals to be operated and tested with the test pattern from the enabled registers.

The feature of "the registers of the present invention are not serially connected to each other" is well supported

As shown in Figure 3 and corresponding description, the MUX finite state machine controller is used to control the test pattern, in a time division way, to be stored in the register 310 coupled to ENR1 signal, to be stored in the register 312 coupled to ENR2 signal, and to be stored in the register 314 coupled to ENR3 signal. The registers 310, 312 and 314 are under control of the MUX finite state machine controller and can not be serially connected to each other. The same disclosure can be found in the Figure 4 and corresponding description in the specification.

Discussion of Office Action Rejection by the Crouch

The Office Action rejected claim 1-11 under 35 U.S.C. 102(b), as being anticipated by Crouch. Applicants respectfully traverse the rejections for at least the reasons set forth below.

First of all, Applicants want to emphasize that the Crouch reference relates to "a full scan test architecture." As disclosed in the Col.6, Lines 1-10, it stats that

> "Once the proper scan system is connected or set-up as discussed above, the tester applies a long serial data vector to the single scan input pin which is accepted by the flip-flops of the selected functional block to be tested in a serial manner while zeros are simultaneously applied to all scan chains in all non-selected functional blocks. While the serial scan vector is being shifted in, the existing state of the scan shift register would be shifted out one bit at a time synchronous to each rising edge of the clock on the single scan output pin, SDO (see FIG. 1).

The Crouch reference does not disclose "providing a test pattern **through a plurality of input lines**", as claimed in claim 1 and claim 6, which is not a serial manner. However, in the Crouch, a long serial data vector is provided through a single scan input pin ("SCAN DATA IN 59", FIG.2).

The Crouch reference does not disclose "sequentially configuring a plurality of registers with the test pattern in a plurality of **different states** according to the test pattern" as claimed in claim 1, also does not disclose "different states **of the multiplexing finite state machine controller**" as claimed in claim 6. In the Office Action, it is asserted that the test controller 10 of FIG.2 of the Crouch is the multiplexing finite state machine controller as claimed and the description of Col.6, Lines 1-9 had disclosed the received test pattern, and the description of Col. 9, Lines 10-14claimed feature. Applicants do not agree with such assertions.

The test controller 10 of FIG.2 of the Crouch can be explained in Col.7, Lines 54-59, referred to FIG.1, which stated that:

> The test controller 10 will activate one of the plurality of scan chains by coupling one of the scan chains in the functional blocks 12-22 to the input STDI through the test

> controller 10. In addition, the one selected scan chain is coupled through the MUX 24 to the output scan chain which lies between the output of MUX 24 and the SDO pin.

The test controller 10 of the Crouch activates one of the plurality of scan chains by coupling one of the scan chains in the functional blocks 12-22 to the input STDI through the test controller 10. As also stated in the Col.7, Lines 54-59 of the Crouch,

> The logic value applied to the TSTADDR pins when the MTM logic value is set to scan mode, will cause the demultiplexor 40 to connect the scan data in pin 59 to be connected to the first scannable sequential element of the selected partition block.

The Crouch reference disclosed "a full scan test architecture", however, in the present invention, the registers are not serially connected to each other, which means that the registers in the present invention is not a Full scan test architecture.

The Crouch reference does not disclose "sequentially configuring a plurality of registers with the test pattern in a plurality of different states according to the test pattern" (emphasis added), instead, test controller 10 is used to couple one of the scan chains in the functional blocks to the input STDI. The test controller 10 is not the multiplexing finite state machine controller, as claimed.

The Crouch reference does not disclose that "after all of the registers are configured with the test pattern, the intellectual product circuit module is operated and tested according to the test pattern from the registers." As referred to the Col.6, Lines 1-10 of the Crouch, it stated that

> "While the serial scan vector is being shifted in, the existing state of the scan shift register would be shifted out one bit at a time synchronous to each rising edge of the clock on the single scan output pin, SDO (see FIG. 1).

It is different from the invention that "after all of the registers are configured with the test pattern, the intellectual product circuit module is operated and tested", as claimed.

For at least the foregoing reasons, Applicant respectfully submits that amended claims 1 and 6 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-5, 7-11 are patently defined over the prior art as well.

Application No.: 10/039,852 **Docket No.: JCLA7022-R**

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-11 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 8/24/2005

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809